IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/054,653	Confirmation No.:	9448
First Named Inventor:	Bulucea, Constantin	Filing Date:	18 January 2002
Group Art Unit:	2814	Examiner:	Farahani, D.
Atty. Docket No.:	NS-5127 US		
Title:	Gate-Enhanced Junction Varactor With Gradual Capacitance Variation		
Assignee(s):	National Semiconductor Corporation		

Mountain View, California
3 May 2005

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97(c) WITH FEE UNDER 37 CFR 1.17(p)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, the document listed on the accompanying substitute PTO Form 1449 is called to the attention of the Examiner for the above patent application. The document, copy enclosed, is cited on page 59 of the specification of the above application.

Citation of the listed document shall not be construed as:

1. an admission that the document is necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

Applicant's Attorney notes that the final Office Action mailed 23 February 2005 is incomplete for the reasons stated in the accompanying Amendment and that the finality of the 23 February 2005 Office Action is to be withdrawn. The status of the above application is to be returned to non-final status. Accordingly, this information disclosure statement is

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submitted under the provisions of 37 CFR 1.97(c). Please charge the information disclosure statement fee of $180 as set forth in 37 CFR 1.17(p) to Deposit Account 502641. This paper is being submitted in duplicate.

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Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Application No.
	NS-5127 US	10/054,653
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	Confirmation No.
Substitute PTO Form 1449	Constantin Bulucea	9448
	Filing Date	Group
	January 18, 2002	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AQ	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOCs," IEDM Technical Digest, December 2001, pages 22.6.1 - 22.6.7
	AR	
	AS	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.